REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1 - 45 are pending. Claims 1, 3, 5, 6, 14, 15, 19, 31, 32, 35, 39, and 43 have been. No claims have been canceled. No claims have been added.

The Examiner objects to Figures 1A, 1B, 3A, 4A, and 5A for minor informalities. Accordingly, Figures 1A, 1B, 3A, 4A, and 5A have been amended based on the Examiner's recommendations. Applicants respectfully re-submit replacement drawing sheets of Figures 1A, 1B, 3A, 4A, and 5A. Withdrawal of the objections is respectfully requested.

The Examiner objects to the abstract of the disclosure because it contains the phrase, "has been disclosed." The abstract has been amended to replace the phrase "has been disclosed" with "has been presented." It is respectfully submitted that the amendment has overcome the objection. Withdrawal of the objection is respectfully requested.

The Examiner objects to the specification because of the following informalities: in paragraph 0051 there is a reference to a Figure 7, whereas there is not such figure in the drawings or the description of the drawings. The reference to Figure 7 has accordingly been corrected to refer to Figure 6A. Withdrawal of the objection is respectfully requested.

The Examiner rejects claim 15 under 35 U.S.C. §112, first paragraph, alleging that the specification, while being enabling for sending a header not contiguously with its respective read data return (shown in Figures 5 and 6 and their explanation), does not reasonably provide enablement for sending the header before the read data return arrives at one of the buffers. The Examiner purports that the specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

The Examiner's attention is respectfully directed to paragraph [0055] and Figure 6C. Paragraph [0055] and Figure 6C include some of the examples of enabling description of the subject matter as claimed in claim 15. Withdrawal of the rejection is respectfully requested.

The Examiner rejects claims 14-15 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has accordingly amended claims 14 and 15 to more particularly point out and distinctly claim the subject matter that Applicant regards as the invention. Withdrawal of the rejection is respectfully requested.

Claims 43-44 were rejected under 35 U.S.C. §102(b) as being anticipated by Dover, U.S. Patent Publication No. 2003/0005239. Applicant respectfully traverses the rejection.

Claim 43 recites:

> ***interleaving*** flits of the non-critical chunks with a plurality of flits of a second cache line ***at the memory controller***; and
>
> if the predetermined number of non-critical chunks have accumulated in the buffer, sending the interleaved flits of the non-critical chunks from the memory controller to the processor.

(Claim 43 as amended; emphasis added)

In contrast, Dover fails to disclose at least the above limitation.

Dover discloses a system having two hosts 100 and 105 (each of which is a processing device) coupled to a memory controller 120 via a bus 110. The memory controller 120 is further coupled to a virtual port memory device 150 via another bus 140. (Dover, Figure 1). The virtual port memory device 150 may transmit data in a time-sliced manner to the memory controller 120 such that words in response to different requests alternate (Dover, paragraphs [0021] and [0040]-[0043]; Figure 4). The memory controller 120 sends critical data to the hosts 100 and/or 105 first, and then combines several responses from the virtual port memory device 150 into a burst response transaction to send to the hosts 100 and/or 105 (Dover, paragraph [0016]). Note that the virtual port memory device

150 transmits data in a time-sliced manner to the memory controller 120 in Dover. The memory controller 120 combines several responses from the virtual port memory device 150 into a burst response transaction to send to the hosts. Dover does not disclose, suggest, or imply ***interleaving flits*** of the non-critical chunks with a plurality of flits of a second cache line ***at the memory controller.*** Therefore, Dover does not disclose at least the limitation of claim 43 set forth above. For at least this reason, Dover does not anticipate claim 43. Withdrawal of the rejection is respectfully requested.

Furthermore, claim 1 sets forth "interleaving ***flits.***" In contrast, Dover discloses transmitting ***words*** in a time-sliced manner from a memory device (Dover, paragraphs [0021] and [0040]-[0043]; Figure 4). Words are distinct and separate from flits. A flit is the granularity at which the link layer of a packetized interconnect sends data. The virtual-port memory device 150 in Dover is not a packetized interconnect. Therefore, the virtual-port memory device 150 in Dover does not transmit flits. For the above reason, Dover does not anticipate claim 43. Withdrawal of the rejection is respectfully requested.

Claim 44 depends from claim 43, and is therefore also not anticipated by Dover for the reason discussed above with respect to claim 43. Withdrawal of the rejection is respectfully requested.

Claims 1-3 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over the alleged applicant's admitted prior art (AAPA), Janzen, U.S. patent application publication 2003/0018845, and Dodd et al., US Patent Application publication No. 2003/0182513. Applicant respectfully traverses the rejection.

Claim 1 as amended sets forth:

> splitting the first read data return into a first plurality of flits and the second read data return into a second plurality of flits;
>
> interleaving the first and the second pluralities of flits to be sent to a processor such that ***one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits.***

(Claim 1 as amended; emphasis added).

As admitted in the Office Action, the alleged AAPA does not disclose interleaving.

As to Janzen, the reference discloses an "interleaved burst mode" for reading a block of data on the same row. To read the block of data, a start address of the block is provided. The remaining addresses are generated by an exclusive OR of the burst start address and an output of an internal counter. (Janzen, paragraphs [0007], [0031], and [0032]). In other words, there is only *one* data return in Janzen, i.e., the block of data, and words within the block of data

are merely reordered in the "interleaved burst mode" in Janzen. Thus, Janzen does not disclose, suggest, or imply interleaving flits of two read data returns.

As to Dodd, the reference discloses interleaving outputs of different memory devices (Dodd, paragraph [0026]). However, the outputs are interleaved on a read return level, that is, all the chunks of a read return are sent before the chunks of the next read return are sent. For example, chunks A0-A3 are sent first, followed by chunks B0-B3, then followed by chunks C0-C3 (see data on external bus in Figures 3, 4, 6, 9, and 10 in Dodd). In other words, the chunks of each read return are sent consecutively without a chunk from another read return getting in between. Thus, Dodd does not disclose interleaving the first and the second pluralities of flits to be sent to a processor such that ***one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits.***

Since none of the alleged AAPA, Janzen, or Dodd, alone or in combination, discloses the limitation set forth above, claim 1 as amended is patentable over the alleged AAPA, Janzen, and Dodd. Withdrawal of the rejection is respectfully requested.

Claims 2-3 and 5 depend from claim 1. Thus, claims 2-3 and 5 are patentable over the alleged AAPA, Janzen, and Dodd. Withdrawal of the rejection is respectfully requested.

Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA, Janzen, Dover, and Dodd. Applicant respectfully traverses the rejection. Claim 4 depends from claim 1, and thus, includes every limitation set forth in claim 1. As discussed above with respect to claim 1, none of the alleged AAPA, Janzen, or Dodd, alone or in combination, discloses interleaving the first and the second pluralities of flits to be sent to a processor such that ***one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits***. Furthermore, Dover fails to make up the deficiencies in the alleged AAPA, Janzen, and Dodd.

Dover discloses transmitting ***words*** in a time-sliced manner from a memory device (Dover, paragraphs [0021] and [0040]-[0043]; Figure 4). Words are distinct and separate from ***flits***. A flit is the granularity at which the link layer of a packetized interconnect sends data. The virtual-port memory device 150 in Dover is not a packetized interconnect. Therefore, the virtual-port memory device 150 in Dover does not transmit flits. As such, Dover also fails to teach interleaving the first and the second pluralities of flits to be sent to a processor such that ***one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits***. Since none of the alleged AAPA, Janzen, Dodd, and Dover discloses every limitation of claim 4,

claim 4 is patentable over the alleged AAPA, Janzen, Dodd, and Dover. Withdrawal of the rejection is respectfully requested.

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over the alleged AAPA in view of Janzen. Applicant respectfully traverses the rejection for the reason discussed above with respect to the rejection of claim 1 under §103(a) as being unpatentable over the alleged AAPA, Janzen, and Dodd. Withdrawal of the rejection is respectfully requested.

Claims 31-42 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and Dodd. Applicant respectfully traverses the rejection.

Claim 31 sets forth:

> interleaving a first plurality of flits containing a first critical chunk of a first cache line and a second plurality of flits containing a second critical chunk of a second cache line, the first and second pluralities of flits corresponding to a first and a second read data returns, respectively, such that one or more flits of the second plurality of flits are ***between*** two consecutive flits of the first plurality of flits.

(Claim 31 as amended; emphasis added)

Dodd discloses interleaving outputs of different memory devices (Dodd, paragraph [0026]). However, the outputs are interleaved on a read return level, that is, all the chunks of a read return are sent before the chunks of the next read return are sent. For example, chunks A0-A3 are sent first, followed by chunks B0-B3, then followed by chunks C0-C3 (see data on external bus in Figures 3, 4, 6,

9, and 10 in Dodd). In other words, the chunks of each read return are sent consecutively without a chunk from another read return getting in *between*. Thus, Dodd does not disclose the limitation set forth above.

As to Dover, the reference discloses transmitting ***words*** in a time-sliced manner from a memory device (Dover, paragraphs [0021] and [0040]-[0043]; Figure 4). Words are distinct and separate from ***flits***. A flit is the granularity at which the link layer of a packetized interconnect sends data. The virtual-port memory device 150 in Dover is not a packetized interconnect. Therefore, the virtual-port memory device 150 in Dover does not transmit flits. As such, Dover also fails to teach the limitation set forth above. Since none of Dover and Dodd discloses the limitation of claim 31 set forth above, claim 31 as amended is patentable over Dover and Dodd. Withdrawal of the rejection is respectfully requested.

For the reason discussed above with respect to claim 31, claims 35 and 39 are patentable over Dover and Dodd. Withdrawal of the rejection is respectfully requested.

Claims 32-34, 36-38, and 40-42 depend from claims 31, 35, and 39, respectively. Thus, for the reason discussed above with respect to claim 31, claims 32-34, 36-38, and 40-42 are patentable over Dover and Dodd. Withdrawal of the rejection is respectfully requested.

Claim 45 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and AAPA. Applicant respectfully traverses the rejection. Claim 45 depends from claim 43, and thus, includes every limitation of claim 43. For the reason discussed above with respect to claim 43, Dover does not disclose every limitation set forth in claim 45. Moreover, the alleged AAPA does not disclose ***interleaving flits*** of the non-critical chunks with a plurality of flits of a second cache line ***at the memory controller***. Since Dover and the alleged AAPA, alone or in combination, do not include every limitation of claim 45, claim 45 is patentable over Dover and the alleged AAPA.

Claims 43-45 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and AAPA. Applicant respectfully traverses the rejection. For the reason discussed above with respect to the other rejections on claims 43 and 45, Dover and the alleged AAPA, alone or in combination, do not include every limitation of claim 45, claim 45 is patentable over Dover and the alleged AAPA.

Claims 6 and 16-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and Blanchard, U.S. Patent No. 5,793,431. Applicant respectfully traverses the rejection.

Claim 6 as amended sets forth:

> a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines,

respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits.

(Claim 6 as amend; emphasis added)

As to Dover, the reference discloses transmitting ***words*** in a time-sliced manner from a memory device (Dover, paragraphs [0021] and [0040]-[0043]; Figure 4). Words are distinct and separate from ***flits***. A flit is the granularity at which the link layer of a packetized interconnect sends data. The virtual-port memory device 150 in Dover is not a packetized interconnect. Therefore, the virtual-port memory device 150 in Dover does not transmit flits. As such, Dover fails to teach the limitation set forth above.

As to Blanchard, the reference discloses two buffers to hold audio and/or video data (Blanchard, col. 7, ln. 45-55). Blanchard does not disclose a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits.

Since none of Dover and Blanchard discloses the limitation of claim 6 set forth above, claim 6 as amended is patentable over Dover and Blanchard. Withdrawal of the rejection is respectfully requested.

Furthermore, Blanchard is directed to encoding of audio and video data while Dover is directed to virtual port memory devices, which are two distinct

and separate technical fields. One of ordinary skill in the art faced with the problem of memory access would not have been motivated to look into Blanchard for possible solution. For this reason as well, claim 6 would not have been obvious over Dover in view of Blanchard. Withdrawal of the rejection is respectfully requested.

Claims 16-18 depend from claim 6. Thus, claims 16-18 are patentable over Dover in view of Blanchard for the reason discussed above with respect to claim 6. Withdrawal of the rejection is respectfully requested.

Claims 7-8 and 10-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and Blanchard, and further in view of AAPA. Applicant respectfully traverses the rejection. Claims 7-8 and 10-14 depend from claim 6, and thus, each includes every limitation of claim 6. For the reason discussed above with respect to claim 6, Dover and Blanchard do not include every limitation of each of claims 7-8 and 10-14. Furthermore, the alleged AAPA does not disclose a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits. Thus, Dover, Blanchard, and the alleged AAPA, alone or in combination, fail to disclose every limitation set forth in each of claims 7-8 and 10-14. For at least this reason, claims

7-8 and 10-14 are patentable over Dover, Blanchard, in view of the alleged AAPA. Withdrawal of the rejection is respectfully requested.

Claim 15 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and Blanchard and AAPA and further in view of Osborne, U.S. Patent Application Publication No. 2003/0093632. Applicant respectfully traverses the rejection. Claim 15 depends from claim 6, and thus, includes every limitation of claim 6. For the reason discussed above with respect to claims 6-8 and 10-14, none of Dover, Blanchard or the alleged AAPA discloses a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits. Furthermore, Osborne merely discloses sending a header before the corresponding read data return starts arriving (Osborne, Fig. 6a; paragraphs [0050]-[0051]). Osborne fails to disclose a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits. Since none of Dover, Blanchard, AAPA, or Osborne, alone or in combination, includes every limitation of claim 15, claim 15 is patentable over Dover,

Blanchard, AAPA, and Osborne. Withdrawal of the rejection is respectfully requested.

Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dover and Blanchard and AAPA and further in view of Hollums, U.S. Patent Application Publication No. 2002/0188905. Applicant respectfully traverses the rejection. Claim 9 depends from claim 6, and thus, includes every limitation of claim 6. For the reason discussed above with respect to claims 6-8 and 10-14, none of Dover, Blanchard or the alleged AAPA discloses a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits. Furthermore, Hollums merely discloses interleaving codewords in a burst (Hollums, para. [0064]-[0066]; Fig. 3d). Hollums does not disclose a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively, such that one or more flits of the second plurality of flits is sent between two consecutive flits of the first plurality of flits. Since none of Dover, Blanchard, AAPA, or Osborne, alone or in combination, includes every limitation of claim 9, claim 9 is patentable over Dover, Blanchard, AAPA, and Hollums. Withdrawal of the rejection is respectfully requested.

Claims 19 and 25-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dover, Dodd and Blanchard. Applicant respectfully traverses the rejection. Claim 19 sets forth:

> a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines, such that one or more flits of the second cache line is sent between two consecutive flits of the first cache line.

(Claim 19 as amended)

As discussed above with respect to claim 6, Dover and Blanchard, alone or in combination, fails to disclose the above limitation. Moreover, Dodd discloses interleaving outputs of different memory devices (Dodd, paragraph [0026]). However, the outputs are interleaved on a read return level, that is, all the chunks of a read return are sent before the chunks of the next read return are sent. For example, chunks A0-A3 are sent first, followed by chunks B0-B3, then followed by chunks C0-C3 (see data on external bus in Figures 3, 4, 6, 9, and 10 in Dodd). In other words, the chunks of each read return are sent consecutively without a chunk from another read return getting in *between*. Thus, Dodd does not disclose the limitation set forth above.

Since Dover, Blanchard, and Dodd, alone or in combination, fail to disclose the limitation of claim 19 set forth above, claim 19 as amended is patentable over Dover, Blanchard, and Dodd. Withdrawal of the rejection is respectfully requested.

Claims 25-30 depend from claim 19. Thus, claims 25-30 are patentable over Dover, Blanchard, and Dodd for the reason discussed above with respect to claim 19. Withdrawal of the rejection is respectfully requested.

Claims 20-21 and 23-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dover, Dodd and Blanchard and further in view of AAPA. Applicant respectfully traverses the rejection. Claims 20-21 and 23-24 depend from claim 19, and thus, each of claims 20-21 and 23-24 includes all the limitations of claim 19. For the reason discussed above with respect to claim 19, Dover, Dodd, and Blanchard, alone or in combination, fail to disclose a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines, such that one or more flits of the second cache line is sent between two consecutive flits of the first cache line. Furthermore, the alleged AAPA does not disclose a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines, such that one or more flits of the second cache line is sent between two consecutive flits of the first cache line. Therefore, claims 20-21 and 23-24 are patentable over Dover, Dodd and Blanchard and further in view of AAPA because Dover, Dodd, Blanchard, and AAPA, alone or in combination, do not disclose every limitation of each of claims 20-21 and 23-24. Withdrawal of the rejection is respectfully requested.

Claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dover, Dodd, Blanchard, AAPA and further in view of Hollums. Applicant respectfully traverses the rejection. Claim 22 depends from claim 19, and thus, claim 22 includes all the limitations of claim 19. For the reason discussed above with respect to claims 19-21 and 23-24, Dover, Dodd, Blanchard, and the alleged AAPA, alone or in combination, fail to disclose a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines, such that one or more flits of the second cache line is sent between two consecutive flits of the first cache line. Furthermore, Hollums merely discloses interleaving codewords in a burst (Hollums, para. [0064]-[0066]; Fig. 3d). Hollums does not disclose a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines, such that one or more flits of the second cache line is sent between two consecutive flits of the first cache line. Therefore, claim 22 is patentable over Dover, Dodd and Blanchard and further in view of AAPA and Hollums because Dover, Dodd, Blanchard, Hollums, and AAPA, alone or in combination, do not disclose every limitation of claim 22. Withdrawal of the rejection is respectfully requested.

CONCLUSION

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the pending claims are in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the pending claims be allowed.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Chui-kiu Teresa Wong
Attorney for Applicant
Reg. No. 48,042

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300